AMENDMENTS TO THE SPECIFICATION

Please amend the **second** paragraph of page 3 as follows:

FIG 1B is a sectional view according to line I-I of FIG 1A. As shown in the drawing, the TFT includes a gate electrode 10 electrically coupled with the gate bus line 2, a gate insulator 10 on a gate electrode 10, an a-Si layer 15 on a gate insulator 13, an n+ a-Si layer 16 on the a-Si layer 15, and source/drain electrodes 17, 18 which are electrically coupled the data bus line 1 and the data electrode 19, respectively. The gate insulator 13 is formed on the inner surface of a first substrate 4. The common electrode 11 is formed with the gate electrode 10 and electrically coupled to the common line 5. Further, a passivation layer 20 and a first alignment layer ~~(not illustrated)~~ (21) are deposited on the inner surface of the first substrate 4.

Please amend the **third** paragraph of page 3 as follows:

On a second substrate 6, a black matrix 7 is formed to prevent a light leakage around the TFT, the data bus line 1, an the gate bus line 2. A color filter later 8, an over-coat layer 9, and a second alignment layer ~~(not illustrated)~~ (22) are formed on the